

SPECIFICATIONS FOR THE NI PXI/PCI-5401

PXI/PCI Arbitrary Function Generator

This document lists the specifications for the NI PXI/PCI-5401. These specifications are typical at 25 °C unless otherwise stated. The operating temperature range is 0–50 °C.

Analog Output

Number of channels	1
Resolution	12 bits
Maximum update rate	40 MHz
DDS accumulator	32 bits
Frequency range	
Sine	16 MHz, max
SYNC (TTL)	16 MHz, max
Square	1 MHz, max
Ramp	1 MHz, max
Triangle	1 MHz, max
Frequency resolution	9.31 MHz

Voltage Output

Ranges	±5 V into a 50 Ω load; ±10 V into a high-impedance load
Accuracy	±0.1 dB
Output attenuation	0–73 dB
Resolution	0.001 dB steps

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Pre-attenuation offset

Range ± 2.5 V into 50Ω ¹

Accuracy ± 5 mV

Output couplingDC

Output impedance 50Ω or 75Ω , software selectable

Load impedance 50Ω or greater

Output enableSoftware switchable

ProtectionShort-circuit protected

Typical rise/fall time8 ns (10–90% 0–5 V square wave
into 50Ω load, filters off)

Sine Spectral Purity

Harmonic products and spurs

Up to 1 MHz–60 dBc

Up to 16 MHz–35 dBc

Phase noise–105 dBc/Hz at 10 kHz
from carrier

Filter Characteristics

Digital

TypeHalf-band interpolating

SelectionSoftware switchable
(enable or disable)

Taps67

Filter coefficientsFixed 20-bit

Data interpolating frequency80 MS/s

Pipeline signal delay26 sampling periods

Analog

Type7th-order L-C lowpass filter

Passband ripple ± 2 dB

¹ With less than 10 dB of attenuation, signal maximum plus offset (before attenuation) must not exceed ± 5 V (into 50Ω).

Waveform Specifications

Memory	16,384 16-bit samples
Segment length.....	16,384 samples, exact
Segment linking (instruction FIFO).....	512 links

Timing I/O

Update clock	Internal, 40 MHz only
Frequency locking	
External reference sources	Input connector, RTSI clock line, or internal
Reference clock frequencies	1 MHz, 5–20 MHz in 1 MHz steps
Frequency locking range.....	±100 ppm

Triggers

Digital Trigger

Compatibility	TTL
Response	Rising edge
Pulse width (T_{d1}).....	20 ns, minimum
Trigger to waveform output delay (T_{d2}).....	28 sample clocks plus 150 ns, max

RTSI

Trigger lines	7
Clock lines.....	1

Bus Interface

Type	Slave
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Operational Modes

Type	Single, continuous, stepped
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SYNC Out

Level	TTL
Duty cycle	20–80%, software controllable

External Clock Reference Input

Frequency	1 MHz or 5–20 MHz in 1 MHz steps
Amplitude	$1 V_{\text{pk-pk}} \leq \text{level} \leq 5 V_{\text{pk-pk}}$

Internal Clock

Frequency	40 MHz
Initial accuracy	± 5 ppm
Temperature stability (0 to 50 °C)	± 25 ppm
Aging (1 year)	± 5 ppm

Mechanical

Connectors

ARB (output)

PCI	SMB
PXI	BNC

SYNC (output)

PCI	SMB
PXI	BNC

PLL reference (input)

.....	SMB
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External trigger in

PCI	50-pin digital
PXI	SMB

Size 1 slot

Power requirements 5 V, 3.5 A, max;
12 V, 125 mA

Safety

Designed in accordance with IEC 61010-1, EN 61010-1, UL 3111-1, and CAN/CSA C22.2 No. 1010.1 for electrical measuring and test equipment.

Electromagnetic Compatibility

EMC/EMI.....	CE, C-Tick, and FCC Part 15 (Class A) Compliant
Electrical emissions.....	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Electrical immunity.....	Evaluated to EN 61326-1:1997 A1:1998, Table 1



Note For full EMC and EMI compliance, you must operate this device with shielded cabling. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at ni.com/hardref.nsf/. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC (in Adobe Acrobat format) appears. Click the Acrobat icon to download or read the DoC.